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TO Convert Based on DC–DC Based on 3SSC and VMC

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Abstract

Proposed on this work as a viable solution to step-up a low battery voltage into a high voltage dc link. This converter is suitable for non-isolated on-line UPS systems with common neutral connection that improves bypass circuit installation. Furthermore, smaller size, higher efficiency, and increased reliability are features that spread the transformer less products. This paper introduces a new family of dc–dc converters based on the three-state switching cell and voltage multiplier cells. A brief literature review is presented to demonstrate some advantages and inherent limitations of several topologies that are typically used in voltage step-up applications. The adopted control strategy uses a hybrid control that implements both analog and digital controllers, that implements the average current mode control. It presents characteristic of continuous input current through the batteries that improve its lifetime, the maximum voltage across the controlled switches is equal to one fourth of the total output voltage, and voltage equalization across the dc-link capacitors is intrinsic. In order to verify the feasibility of this topology, principle of operation, theoretical analysis, and experimental waveforms are shown for a 1.55 kW assembled prototype. proposed on this work as a viable solution to step-up a low battery voltage into a high voltage dc link. This converter is suitable for non-isolated on-line UPS systems with common neutral connection that improves bypass circuit installation. Furthermore, smaller size, higher efficiency, and increased reliability are features that spread the transformer less products. The adopted control strategy uses a hybrid control that implements both analog and digital controllers, that implements the average current mode control. It presents characteristic of continuous input current through the batteries that improve its lifetime, the maximum voltage across the controlled switches is equal to one fourth of the total output voltage, and voltage equalization across the dc-link capacitors is intrinsic. The analyzed converter can be applied in uninterruptible power supplies, fuel cell systems, and is also adequate to operate as a high-gain boost stage with cascaded inverters in renewable energy systems. Furthermore, it is suitable in cases where dc voltage step-up is demanded, such as electrical fork-lift, audio amplifiers, and many other applications.

Keywords: Boost converters, dc–dc converters, and high voltage gain, voltage multiplier cells (VMCs).

Introduction

Uninterruptable power supply (UPS) systems are employed to supply critical loads with continuous and high quality energy in facilities such as hospitals, data centers, and communication systems etc [1]. Among the different on-line UPS topologies, the transformer less UPS presents higher efficiency due to the absence of the isolation transformer that increases considerably the size/weight of the overall system [2]. The overall advantages of modern transformer less UPS systems over those with isolation transformer (which are now considered obsolete) can be summed up and summarized as input-output power quality enhancement, lower operating and energy cost with high return on investment on the new technology UPS, and significantly enhanced reliability The conventional boost converter can be advantageous for step-up applications that do not demand very high voltage gain, mainly due to the resulting low conduction loss and design simplicity. Theoretically, the boost converter static gain tends to be infinite when duty cycle also tends to unity. However, in practical terms, such gain is limited by the I2R loss in the boost inductor due to its intrinsic resistance, leading to the necessity of accurate and high-cost drive circuitry for the active switch, mainly because great variations in the duty cycle will affect the output voltage directly Cascading one or more boost converters may be considered to obtain high voltage gain. Even though more than one power processing stage exists, the operation in continuous conduction mode (CCM) may still lead to high efficiency [9]. The main drawbacks in this case are increased complexity and the need for two sets that include active switches, magnetic, and controllers. Besides, the controllers must be synchronized and stability is of great concern [10]. Due to high power levels and high output voltage, the latter cascaded boost stage has severe reverse losses, with

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consequent low efficiency and high electromagnetic interference (EMI) levels. Typical examples of such topologies are the single-switch quadratic boost converter and the two-switch three-level boost converter [11]. Converters with magnetically coupled inductance such as fly back or the single-ended primary inductance converter (SEPIC) can easily achieve high voltage gain using switches with reduced on-resistance, even though efficiency is compromised by the losses due to the leakage inductance [12]. An active clamping circuit is able to regenerate the leakage energy, at the cost of increased complexity and some loss in the auxiliary circuit [13]. A hybrid boost–fly back converter is introduced in [14]. The efficiency of the conventional fly back structure is typically low due to the parasitic inductance. A possible solution lies in connecting the output of the boost converter to that of the fly back topology, with consequent increase of voltage gain due to the existent coupling between the arrangements. In this case, the boost convert behaves as an active clamping circuit when the main switch of the fly back stage is turned OFF.

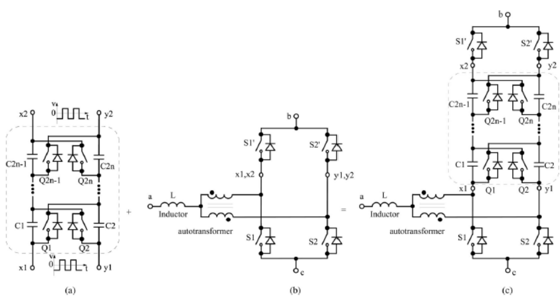


Fig 1 (a) Voltage multiplier cell (b) Three-state swithing cell (c) Resulting cell

Principle of Operation

In order to explain the principle of operation of this converter, it is analyzed in the continuous conduction mode (CCM) operation, with a duty cycle value of the switches higher than 0.5. For this purpose, the semiconductors and magnetic elements are considered ideals. During one commutation period of the converter operation, it presents four operating intervals that are described as follows, and its main theoretical operation waveforms are shown in Fig. 2.

A. First Interval (t0, t1): The switches S1 and S2 are turned on. The energy is stored only in the inductor Lb and is not transferred to the load. All the rectifier diodes are reverse biased in this interval. This interval circuit is represented in Fig. 3.a.

B. Second Interval (t1, t2): In this interval the switch S2 remains turned on. The voltage across switch S1 is equal to the voltage across capacitor C2. The diodes D1, D3, D5 and D8 are directly biased. The energy stored in the inductor in the first interval, as well as the energy from the voltage source are transferred to the filter capacitors C1, C2, C3, and C4. The interval circuit is shown in Fig. 3.b.

C. Third Interval (t2, t3): This interval is similar to the first one, where switches S1 and S2 are turned on, and the energy is only stored in the inductor Lb. The interval circuit is shown in Fig. 3.c.

D. Fourth Interval (t3, t4): During this interval, the switch S1 remains turned on. The voltage across switch S2 is equal to the voltage across the capacitor C2. The diodes D2, D4, D6 and D7 are directly biased. The energy stored in the inductor during the third interval, as well as the energy from the voltage source are transferred to the filter capacitors C1, C2, C3, and C4. The interval circuit is shown in Fig. 3.d.

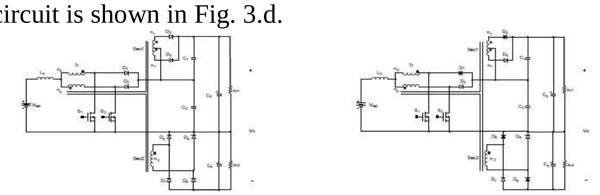
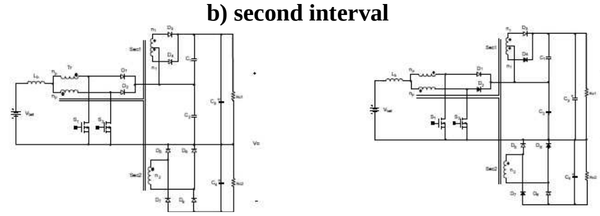


Fig 2.0 a) first Interval
b) second interval



C) third interval
d) fourth interval

Theoretical Analysis

A. Static Gain

The output-input voltage ratio, named as static gain of the converter, is given by (1). In order to get the equal voltage
Values across output capacitors C3 and C4, the transformer turns ratio must respect the relation $n2 = n1 + 2np$.

$$G_V = \frac{V_o}{V_{bat}} = \frac{1}{(1-D)}\left(1 + \frac{n_1}{2 \cdot n_p} + \frac{n_2}{2 \cdot n_p}\right) \qquad (1)$$

Where Vo is the output voltage, Vbat is the battery input voltage, *np* is the primary number of turns, *n*1 is the secondary
1 number of turns, *n*2 is the secondary 2 number of turns and *D* is the duty cycle.

B. Inductor Design

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The current ripple on the storage inductor can be determined using

$$\Delta I_{Lb} = \frac{(2D-1)(1-D)V_o}{2f_s\left(1+\frac{n_1}{2\cdot n_p}+\frac{n_2}{2\cdot n_p}\right)L_b} \qquad (2)$$

In (2), ΔILb is the current ripple on the inductor Lb, and fs is the switching frequency of the converter. Rearranging the terms in (4), the normalized current ripple on the inductor is given by

$$\overline{\Delta I_{Lb}} = \frac{2\Delta I_{Lb}L_b f_s\left(1+\frac{n_1}{2\cdot n_p}+\frac{n_2}{2\cdot n_p}\right)}{V_o} = (2D-1)(1-D) \quad (3)$$

Fig. 4, which was obtained from (3), shows the normalized current ripple on the inductor as a function of the duty cycle. the current ripple, it is possible to calculate the inductor value using

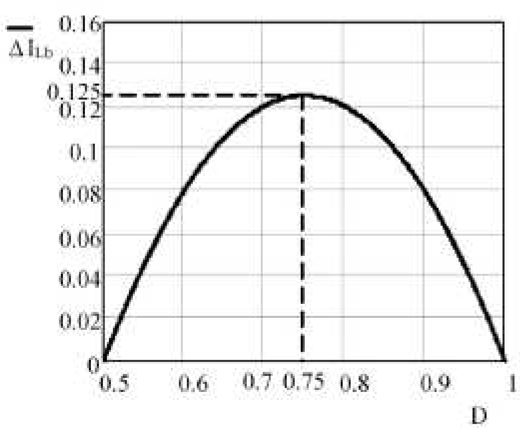
$$L_b = \frac{V_o}{16f_s\left(1+\frac{n_1}{2\cdot n_p}+\frac{n_2}{2\cdot n_p}\right)\Delta I_{Lb}} \qquad (4)$$

C. Transformer Design

The high frequency transformer must be designed accordingly to the amount of power processed given by

$$P_p = \frac{V_{C_1}+0.5\cdot V_{C_2}+V_{C_4}}{V_{C_1}+V_{C_2}+V_{C_4}}P_o \qquad (5)$$

where Pp is the power processed by the transformer, VC1, VC2 and VC4 are the voltages across the capacitors C1, C2 and C4, respectively, and, Po is the output power of the converter.



Experimental Results

A. Specifications

In order to verify the operation and evaluate the performance of the proposed boost converter, a prototype with the specifications shown in Table I was assembled and tested.

TABLE I
Specifications of the Non-Isolated DC-DC Converter using TSSC

Input Voltage Range	V_{bat}	63 - 81 [V_{DC}]
Output Power	P_o	1.55 [kW]
Output Voltage	V_o	710 [V]
Switching Frequency	f_s	40 [kHz]

current ripple max 0.30 *Lb bat ΔI = I* , the voltage across capacitor C2 2 200 *CV = V* , the maximum fixed duty cycle of the switches *Dmax = 0.689* for the minimum input voltage, and the output voltage ripple ΔVo=0.02Vo.

B. Simplified Design Example

The boost inductor is obtained according to (4), substituting values in it is equal to

$$L_b = \frac{700}{16\cdot 40000\cdot\left(1+\frac{18}{2\cdot 12}+\frac{42}{2\cdot 12}\right)\cdot 8.46} = 31.2\mu H .$$

The transformer was built using the push-pull DC-DC converter guidelines for the power rating obtained by (5). Thus,

$$P_p = \frac{(152.5+0.5\cdot 202.5+355)}{(152.5+202.5+355)}\cdot 1550 = 1328.9W .$$

C. Experimental Waveforms and Curves

Figures 5 and 6 shows the battery bank voltage *Vbat* and Mcurrent through the boost inductor *Lb* under nominal load and minimum input voltage conditions. As can be seen, the current drawn by the proposed converter presents a low current ripple, suitable for battery powered applications. Figure 7 shows the drain-to-source voltages across the controlled switches S1 and S2. As can be seen, it is clamped in almost the output filter capacitor C2 voltage, as expected in the theoretical analysis.

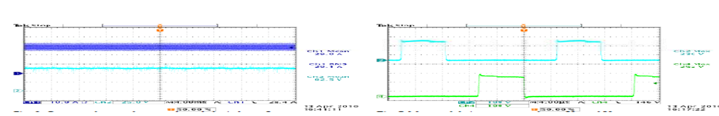


Fig 4.0 Battery voltage and current through the inductor Lb.

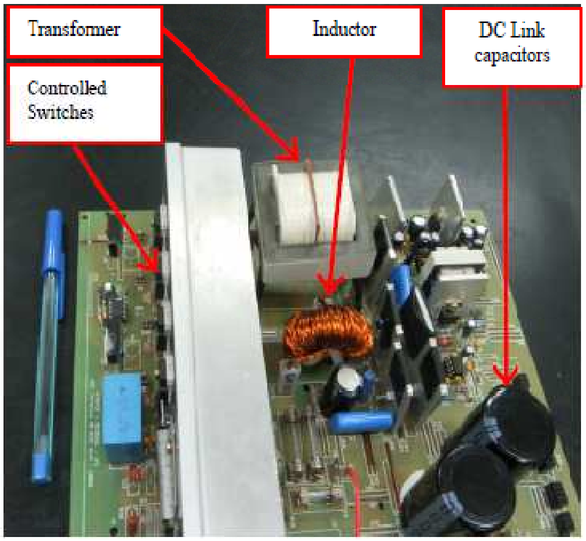


Fig 4.1 Picture of the assembled protocol

Conclusions

This paper proposes a new non-isolated boost converter with a high voltage gain for non-isolated on-line UPS with Common neutral point. Also, the proposed converter can be used for the development of stand-alone systems, and grid connected systems for renewable energies applications. As shown in the experimental results shown in Figs. 5 to 9, it has the following features: a non-pulsated input current that improves the battery lifetime, the voltage across the controlled switches is one fourth of the total output voltage and the voltage across the dc-link filter capacitors are
Naturally balanced even if unbalanced loads is connected. The efficiency curve shown in Fig. 9 confirms such proposal viability for its desired application or others.

References

[1] J. M. Guerrero, L. G. Vicuna, J. Uceda, "Uninterruptible power supply systems provide protection," *IEEE Ind. Electron. Magazine*, vol. 01, no. 1, pp. 28-38, Spring 2007.

[2] R. Koffler, "Transformer or transformerless UPS?" IEE Power Eng. Journal, Vol. 17, no. 3, pp. 34-36, 2003.

[3] I. Gunes, B. Ustuntepe, A. M. Hava, "Modern Transformerless Uninterruptable Power Supply (UPS) Systems", *in International Conference on Electrical and Electronics Engineering*, 2009, ELECO 2009, Vol. 1, pp. I-316 - I-320.

[4] Qun Zhao, Fengfeng Tao, Yougxuan Hu, and Fred C. Lee, "DC/DC Converters Using Magnetic Switches", *in IEEE Applied Power Electronics Conference and Exposition*, 2001, APEC2001, Vol.2, 4-8 March 2001, pp. 946-952.

[5] Qun Zhao, and Fred C. Lee. "High-Effiency, High Step-Up DC-DC Converters", *in IEEE Transactions on Power Electronics*, Vol. 18, No1, January 2003, pp. 65-73.

[6] Yungtaek Jan, and Milan M. Jovanovic. "A New Two-Inductor Boost Converter with Auxiliary Transformer", *in IEEE Transactions on Power Electronics*, Vol. 19, No1, January 2004, pp. 169-175.

[7] Roger Gules, L. Lopes Pfitscher, and L. Claudio Franco. "An Interleaved Boost Dc-Dc Converter with Large Conversion Ratio", *in IEEE International Symposium on Power Electronics*, 2003. ISIE´03, Vol.1, 9-12 June 2003, pp. 411-416.

[8] K. C. Tseng and T. J. Liang, "Novel high-efficiency step-up converter", *in IEE Proc. Electr. Power Appl.*, Vol. 151, No.2, March 2004, pp. 182-190.

[9] R. J. Wai and R. Y. Duan, 'High-efficiency DC/DC converter with high voltage gain", *in IEE Proc. Electr. Power Appl.*, Vol. 152, No.4, July 2005, pp. 793-802.

[10] J. W. Baek. M. H. Ryoo, T. J. Kim, D. W. Yoo, and J. S. Kim, "High Boost Converter Using Voltage Multiplier", *in IEEE Industrial Electronics Conference*, 2005, pp.567-572.

[11] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Transformerless DC-DC Converters with a very High DC Line-to-Load Voltage Ratio", *in Proc. of the 2003 International Symposium on Circuits and Systems*, 2003, ISCAS´03, Vol.3, 25-28 May 2003, pp. III-435 - III-438.

[12] O. Abutbul, A. Gherlitz, Y. Berkovich, and A. Ioinovici, "Step-Up Switching-Mode Converter with High Voltage Gain Using a Switched-Capacitor Circuit", *in IEEE Transactions on Circuits and Systems – I:Fundamental Theory and Applications*, Vol. 50, No.8, August 2003, pp.1098-1102.

[13] Grover V. Torrico Bascopé, and Ivo Barbi. "Generation of a Family of Non-Isolated Dc-Dc PWM Converters Using New Three-State Switching Cells", *in IEEE Power Electronic Specialists Conference*, 2000, PESC'00, Vol.2, 18-23 June 2000, pp. 858-863.

[14] G. V. Torrico-Bascopé, "New Family of Non-isolated DC-DC PWM Converters Using the Three-State Switching Cell", *Ph.D. thesis*, Dept. Elect. Eng., Federal University of Santa Catarina, Brazil, 2001.